[PDF] Baring it all to software: the **raw machine**
E Waingold, M Taylor, V Sarkar, W Lee, V Lee, J Kim, M ... - IEEE computer, 1997 - Citeseer
... IMEM DMEM REGS ALU CL SMEM SWITCH PC PC Static Data **Processor** Code Switch Code Figure 9: Compiler interaction with the architecture ... **Partitioning** into Logical Threads The **Partitioning** phase generates **parallel** code for an idealized **Raw machine** with the ...
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Space-time scheduling of instruction-level parallelism on a **raw machine**
W Lee, R Barua, M Frank, D Srikrishna, J ... - ACM SIGPLAN ..., 1998 - portal.acm.org
... First, it describes the space-time scheduling of ILP on a **Raw machine**, borrow- ing some techniques from the **partitioning** and scheduling of tasks on MIMD machines. ... The network interface on a **Raw machine** is integrated directly into the **processor** pipeline to support ...
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[PDF] **Parallel** and distributed association mining: A survey
MJ Zaki - IEEE CONCURRENCY, 1999 - Citeseer
... is provided on each **processor**, and the hardware or software ensures cache-coherence, ie, making sure that locally cached data always reflects the latest modification by any **processor**. ... It also serves as the base algorithm for the vast majority of **parallel** algorithms. ... 3.3 **Partition** ...
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[CITATION] The MIT Alewife **machine**: Architecture and performance
A Agarwal, R Bianchini, D Chaiken, KL Johnson, D ... - ..., 1995. Proceedings. 22nd ..., 1995
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Maximizing parallelism and minimizing synchronization with affine **partitions**
AW Lim, MS Lam - **Parallel** Computing, 1998 - Elsevier
... In this paper, the SPMD code we show assumes each **processor partition** is mapped to a physical **processor**. To generate code for a specific number of processors, we can simply combine multiple **parallel** threads and assign them to the same **processor**. ...
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[CITATION] The AIS-5000 **parallel processor**
LA Schmitt, SS Wilson, AIS Inc, A Arbor - ... on Pattern Analysis and **Machine** ..., 1988
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A new model for integrated nested task and data **parallel** programming
J Subhlok, B Yang - ... on Principles and practice of **parallel** ..., 1997 - portal.acm.org
... A high level task and data **parallel** implementation of this pipeline is shown in Figure 2(c). The TASK-**PARTITION** statement is ... ON SUBGROUPdirectives are used to map the computations, ie, the three subroutines Cffts , rf f ts and hi st, onto the three **processor** subgroups. ...
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[CITATION] The **RAW** benchmark suite: computation structures for general purposecomputing
J Babb, M Frank, V Lee, E Waingold, R Barua, M Taylor ... - FPGAs for Custom ..., 1997
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A static performance estimator to guide data **partitioning** decisions
V Balasundaram, G Fox, K Kennedy, U ... - ACM Sigplan Notices, 1991 - portal.acm.org
... I **raw**.data **...** of data **partitioning** schemes will depend not only on the nature of data dependence in the program, but also on several target **machine** specific parame **...** This local data is stored within each **processor's** local memory as an **array** val(O:idim+l, O:jdim+l). The interior of the **...**
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[CITATION] A highly parameterizable **parallel processor array** architecture
D Kissler, F Hannig, A Kupriyanov, J Teich - IEEE International Conference on Field ..., 2006
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A General Purpose **Xputer** Architecture derived from DSP and Image Processing
A Ast, RW Hartenstein, H Reinig, K ... - ... for digital signal ..., 1994 - books.google.com
... Xputers (Fig. 7a) have a reconfigurable ALU (rALU), partly using the technology of field-programmable logic. Fig. 7a shows an example: the rALU of the MoM-4 **Xputer** architecture. The four smart **register** files called scan caches are explained later (lower left side in Fig. 7a). ...
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[BOOK] A partitioning compiler for computers with **Xputer**-based accelerators
J Becker - 1997 - Citeseer
Page 1. A Partitioning Compiler for Computers with **Xputer**-based Accelerators by Jürgen Becker Page 2. II Page 3. Page 4. A Partitioning Compiler for Computers with **Xputer**-based Accelerators Jürgen Becker Vom Fachbereich ...
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An operating system for custom computing machines based on the **Xputer** paradigm
R Kress, R Hartenstein, U Nageldinger - Field-Programmable Logic and ... - Springer
... The status of an **Xputer** module consists of much more data: • the current status of the data sequencer, consisting of the current configuration as well ... comprises the current configuration (ranges from 20 to 100 kbits for 96 DPUs), as well as the status of every used **register** in each ...
Cited by 16 - Related articles - BL Direct - All 3 versions

Data-procedural Languages for FPL-based Machines
A Ast, J Becker, R Hartenstein, R Kress, H Reinig, K ... - Field-Programmable Logic ... - Springer
... Throughout this paper, however, we use an **Xputer** architecture supported by smart **register** files, which provide a 2-dimen- sional scan windows (eg figure 2b shows one of size 2-by-2). A scan window gives Page 3. 185 -.•x Legend: • starting Y =ocation I~="~ final "~" location ...
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[PDF] A Two-level Co-Design Framework for **Xputer**-based data-driven reconfigurable Accelera
RW Hartenstein, J Becker - PROCEEDINGS OF THE HAWAII ..., 1997 - Citeseer
... windows look at local segments of memory space, and are part of a smart **register** file interfacing primary memory. Many applications require iterating the same data manipulations on a large amount of data, eg statement blocks in nested loops. The **Xputer** machine paradigm ...
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XMDS: The **Xputer** Multimedia Development System
C Schreiber - Proceedings of the Thirty-Second Annual Hawaii ..., 1999 - portal.acm.org
Google, Inc. (search), Subscribe (Full Service), **Register** (Limited Service, Free), Login. Search: The ACM Digital Library The Guide. ... XMDS: The **Xputer** Multimedia Development System. Full text, Publisher Site Publisher Site. Source, ...

[CITATION] 5.2 A Novel Compilation Technique for a Machine Paradigm Based on Field-Programmable Logic
RVV Hartenstein, K Schmidt, H Reinig, M Weber - FPGAs, 1991 - Abingdon EE&CS Books
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A novel paradigm of parallel computation and its use to implement simple high performance hardware
R Hartenstein, A Hirschbiel, M Weber - CONPAR 90—VAPP IV - Springer
... 2 a), xputers are data-driven (fig. 2 d). Let's illustrate the role of this data sequencer by the MoM **xputer** architecture example featuring a 2-dimensional data address space (fig. 3 b - f). The MoM has 4 **register** files which we call scan windows or scan caches (fig. ...
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[PDF] **Xputer** Module
X Module - 1993 - Citeseer
... The **Xputer** paradigm provides several advantages: The combinations of several operations to one compound operator allow to introduce pipelining and fine ... Intermediate results can be passed along in the pipeline, instead of writing them back into the **register** file after every ...
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[PDF] A partitioning programming environment for a novel parallel architecture
R Hartenstein, J Becker, M Herz, R Kress, U ... - International Parallel ..., 1996 - Citeseer
... is buffered in a scan window (SW), which is a kind of smart **register** file, the location sequence of which in memory space is determined by a data sequencer. All data in the scan windows can be accessed in parallel by the rALU. Each of up to seven **Xputer** modules run ...
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